What is claimed is:

1. A magnetoresistive random access memory comprising a vertical structure field effect transistor,

wherein the vertical structure field effect transistor has its channel column and drain area sequentially formed on an insulation substrate, its source area formed on the insulation substrate on which the channel column has not been formed, and its read word lines formed around the channel column to serve as a gate,

a contact line, a magnetic tunnel junction cell, a bit line and a write word line are sequentially formed on the drain area, and

patterns of the magnetic tunnel junction cell are formed according to a self-alignment method, without requiring a special mask process for forming the patterns.

2. The magnetoresistive random access memory of claim 1, wherein the magnetic tunnel junction cell is aligned in the matrix shape through the self-alignment method by using the bit line and word line masks.

3. The magnetoresistive random access memory of claim 1, wherein the source area and the drain area are formed according to ion implantation, and the channel column is

comprised of silicon.

4. The magnetoresistive random access memory of claim 1, wherein the read word line is formed by depositing polysilicon.

5. The magnetoresistive random access memory of claim 1, wherein the magnetic tunnel junction cell is formed by sequentially stacking a anti-ferroelectric thin film, a pinned ferromagnetic thin film, an insulation layer and a free ferromagnetic thin film on the contact line.

6. A manufacturing method of a magnetoresistive random access memory, comprising:

a first process for forming a vertical structure field effect transistor by sequentially forming a channel columns and a drain area on an insulation substrate, a source area on the insulation substrate on which the channel columns have not been formed, and read word lines around the channel columns serving as gates ;

a second process for forming a magnetic tunnel junction cell and a bit line on the vertical structure field effect transistor, and patterning the magnetic tunnel junction cell according to a self-alignment method aligning the magnetic tunnel junction cell in a matrix shape, by

using the bit line and read word line masks; and

a third process for patterning and etching a write word line on the bit line in the right angle direction to the bit line.

7. The method of claim 6, wherein the first process comprises the steps of:

forming a gate oxide film on the whole surfaces of the drain area and the source area, depositing the read word line, and performing a planarization process thereon;

depositing a first interlayer insulation film on the read word line, and forming a plurality of contact holes on the first interlayer insulation film; and

depositing a contact line on the whole surface to fill the plurality of contact holes.

8. The method of claim 6, wherein the source area and the drain area are formed according to ion implantation, and the channel column is comprised of silicon.

9. The method of claim 6, wherein the read word line is formed by depositing polysilicon.

10. The method of claim 6, wherein the magnetic tunnel junction cell is formed by sequentially stacking a anti-

ferroelectric thin film, a pinned ferromagnetic thin film, an insulation layer and a free ferromagnetic thin film on the contact line.

11. The method of claim 6, wherein the bit line is formed by depositing a metal line on the whole surface.

12. The method of claim 6, wherein the second process comprises the steps of:

forming the magnetic tunnel junction cell on the whole surface of the contact line, and patterning first photoresist on the magnetic tunnel junction cell;

performing an etching process by using the first photoresist to expose the side surfaces of the read word line;

depositing a second interlayer insulation film on the whole surface, performing a planarization process thereon, and depositing the bit line on the whole surface;

patterning second photoresist on the bit line in the right angle direction to the read word line; and

performing an etching process by using the patterned second photoresist to expose the contact line.

13. The method of claim 6, further comprising the step for depositing a third interlayer insulation film on the

whole surface of the bit line prior to the third process.